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DSM-DIRECTED CHIP DESIGN AND VERIFICATION

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Keywords: integrated circuit, design, verification, DSM, DMM, MDM, virtual clustering, degree of diagonality

1 INTRODUCTION

The current approach to integrated circuit (I.C.), or chip, design is not always optimum in terms of "Design-for-Layout". Ideally, it is good practice to create the design schematics and layout so that a one-to-one correspondence exists at all levels of the schematic/layout hierarchy. Instead, the current approach can be somewhat adhoc and therefore prone to non-optimum schematic/layout hierarchy creation, resulting in inefficient development execution.
In addition, the current approach is limited in that it typically does not try to systematically optimise the project (sub-)team members' participation in terms of sub-block interface design and verification. This can result in simulation blindspots or omissions.
We can use the Design Structure Matrix (DSM) [1] and Domain Mapping Matrices (DMM) [2], in a Multi Domain Mapping (MDM) methodology [3], to (i) ensure optimised schematic/layout hierarchy creation and (ii) determine a more optimum configuration of (sub-)team members and design/verification tasks, in a visually powerful way.
DSM-directed chip design and verification should be more efficient and of higher quality, as a consequence.
The DSM has been applied to chip development in the past in the context of activity- or task-based DSMs, using sequencing techniques [4] [5]. The application suggested here involves component- and team-based DSMs, using clustering techniques.

2 CURRENT CHIP DESIGN & VERIFICATION APPROACH AND LIMITATIONS

2.1 Design & Layout

The current chip design and layout approach can be non-optimum. Design engineers can create the schematics in a hierarchy, without consideration for the layout. Layout engineers can create the layout in a hierarchy, without consideration for the design. As a result, the design/layout can be time-consuming to create and verify (from a layout-versus-schematic, or LVS, perspective) successfully.
The current chip design and layout approach is limited in that it does not systematically ensure an extensive as possible one-to-one correspondence between schematic and layout blocks. This is not surprising in that usually design engineers create schematics primarily to support design simulations, without due regard for layout creation.

2.2 Design & Simulation Verification

The current chip design and verification approach can be non-systematic and adhoc. People are (usually) assigned to design/check their own block and the design/verification team structure tends not to take the chip structure into account. As a result, the toplevel simulation checklist can be too limited.
The current chip design and verification approach is limited in that it does not systematically define the simulations to be done, the (sub-)teams to be involved and it does not focus enough at the toplevel.
This is not surprising in that engineers tend to focus in on their own block or area of work, without stepping back to view the overall picture.

3 NEW CHIP DESIGN & VERIFICATION APPROACH AND BENEFITS

The suggested new chip design and verification approach, in terms of both design/layout and design/verification uses an MDM strategy.

3.1 Design & Layout

The suggested new chip design and layout methodology uses an MDM approach, as illustrated in Figure 1.

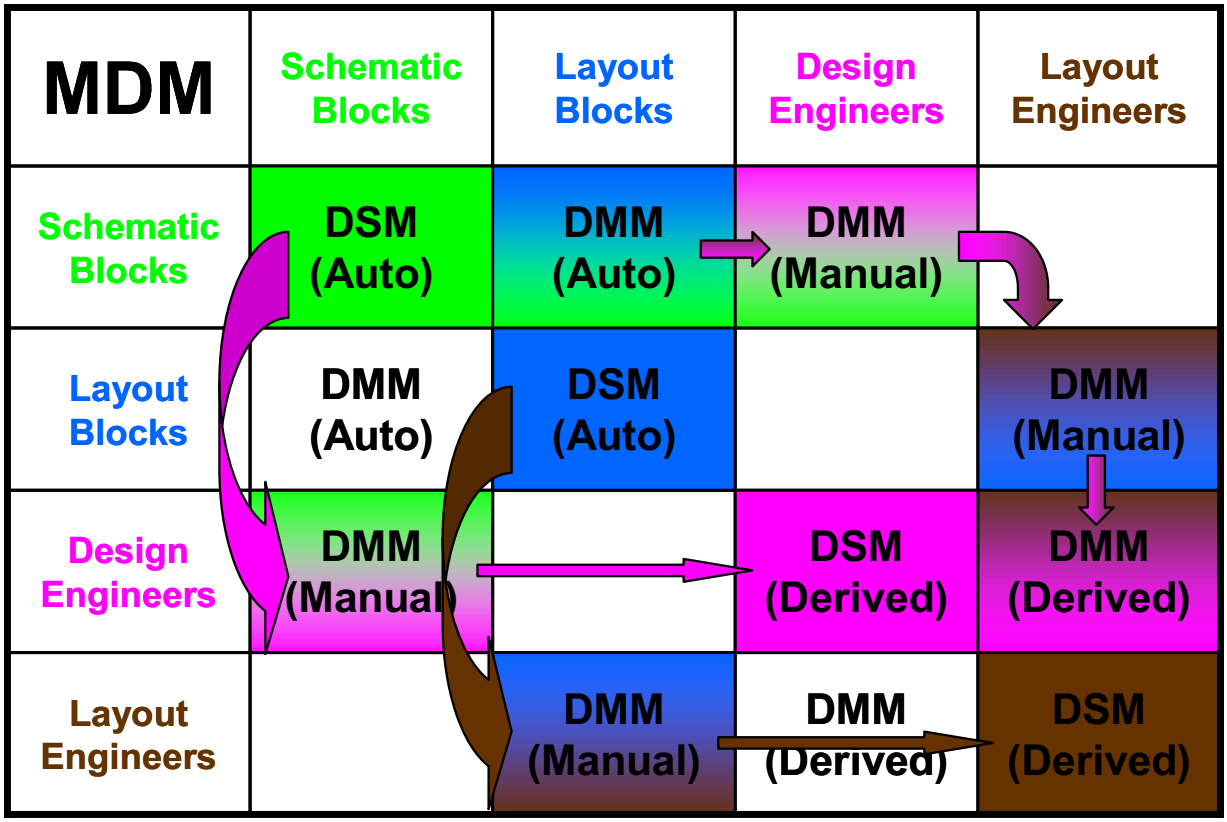

Figure 1. Chip Design & Layout MDM

Schematic Block - Schematic Block DSM and Layout Block - Layout Block DSM

A Schematic Block – Schematic Block DSM would illustrate the degree of connectivity between the schematic blocks.

The connectivity between schematic blocks could be "weighted" by, not only the number of connections, but also by the probability and resultant impact of a problem occurring with those connections.

A Layout Block – Layout Block DSM would illustrate the degree of connectivity between the layout blocks.

Ideally, both of these DSMs should be automatically generated.

Clustering of these DSMs could suggest a better hierarchy for the schematics and layout.

In cases where you don't want to change the current schematic or layout hierarchy, a new approach could be used, called "virtual clustering" (or virtual partitioning), as illustrated in Figure 2.

In the latter, the current hierarchy is not changed but schematic/layout elements that are outside the cluster of immediate interest would be "black-boxed".

In most cases, it is desirable that "black-boxing" should not involve totally empty boxes but instead boxes where each pin (on the box) could be stimulated or monitored.

This "virtual clustering" and "black-boxing" could be automated and the key benefit of this technique would be reduction in the size of the schematic/layout data for more efficient verification analysis, without the need to re-architect the schematic/layout hierarchy.

This methodology could be classified as being in the category of "Design-for-Verification".

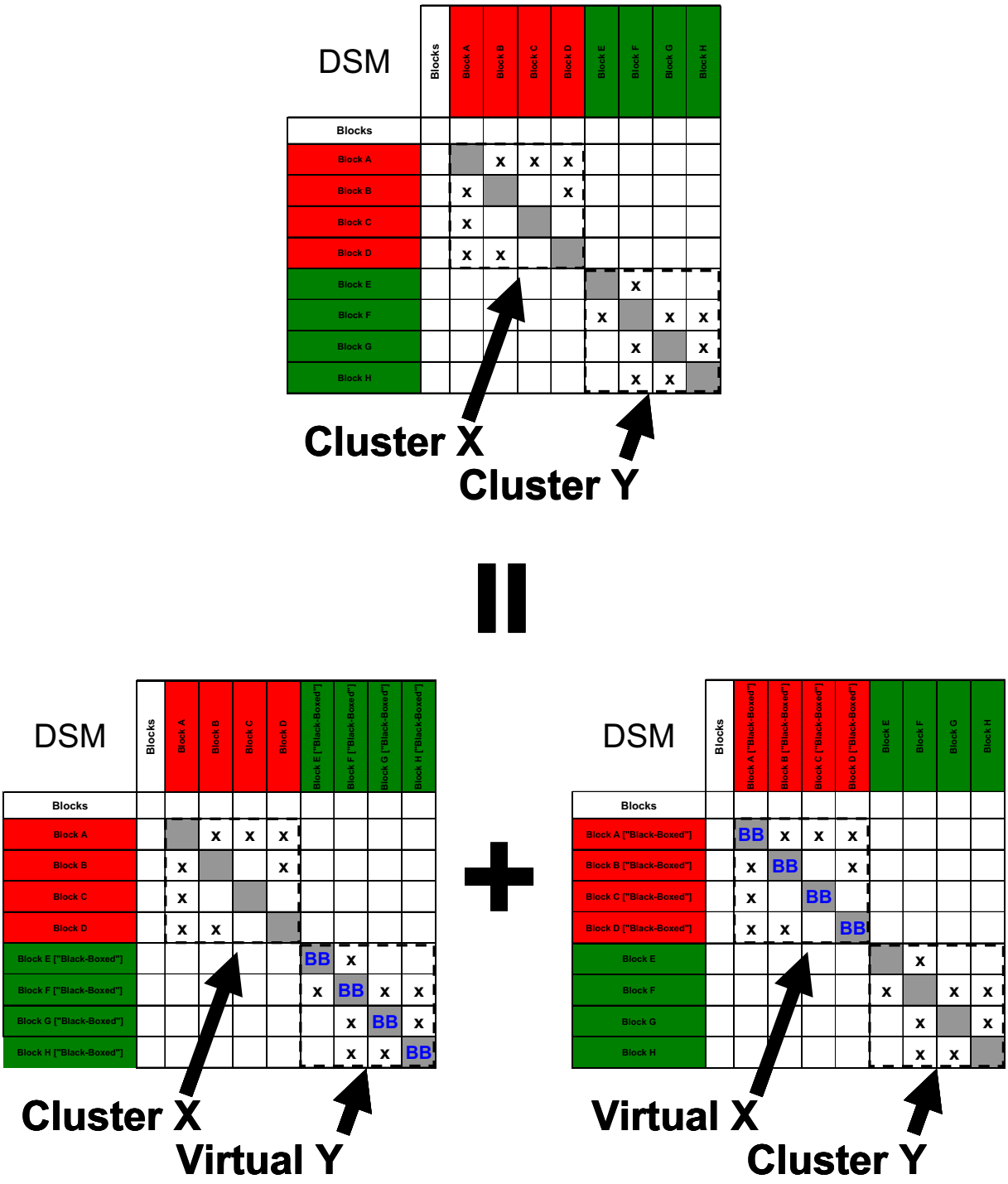

Figure 2. "Virtual" Clustering (or Partitioning)

Schematic Block – Layout Block DMM

A Schematic Block – Layout Block DMM would show the degree of correspondence between schematics and layout blocks/cells in the database hierarchy, an example of which (containing 2,291 blocks) is illustrated in Figure 3. Such a DMM, which could be generated automatically, should ideally be mostly diagonal, indicating a one-to-one relationship between a schematic block and its corresponding layout cell.

Having a design/layout database where each block has both a schematic and layout view is deemed "good practice".

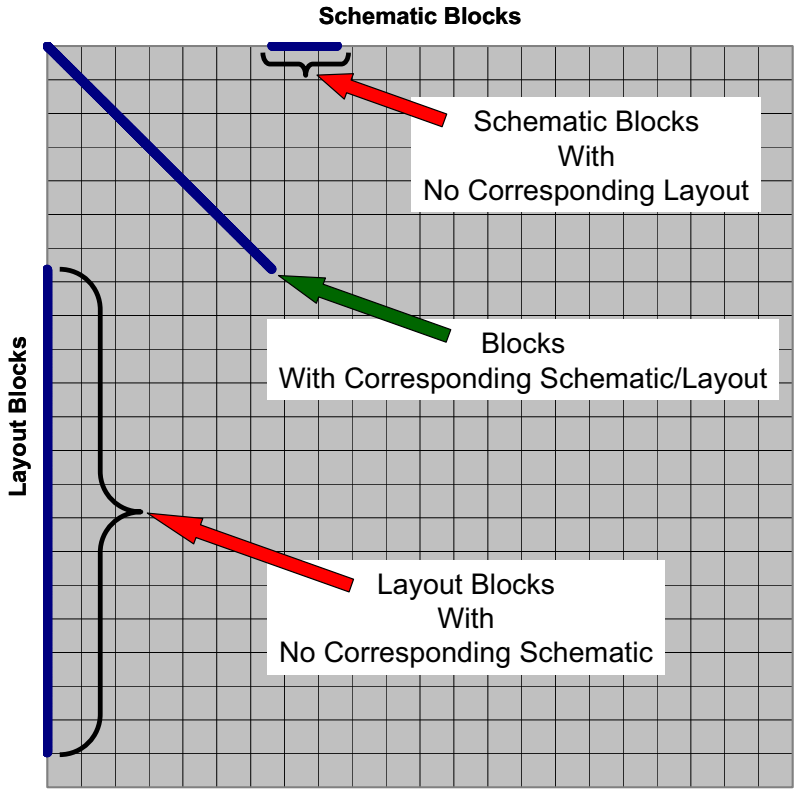

Figure 3. Schematic Block – Layout Block DMM

A re-ordering (and clustering) of the rows/columns of the DMM by hierarchy should result in a complete diagonal in the top-left section of the matrix. Gaps in the diagonal mean no correspondence. An example of a Schematic Block – Layout Block DMM (with 1,152 blocks) is shown in Figure 4.

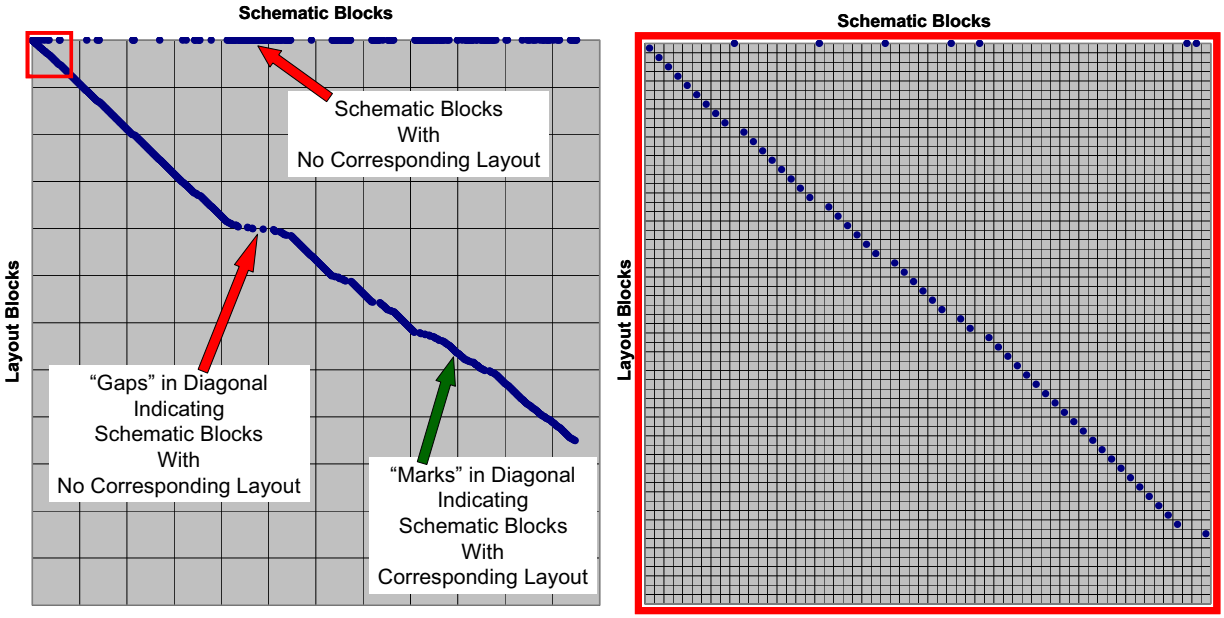

Figure 4. Hierarchical Schematic Block – Layout Block DMM (with zoom-in)

There are potentially two methods of extracting/generating this Schematic Block – Layout Block DMM:

(i) by parsing a design/layout block/cell library hierarchically for schematic and layout views (note that this does not necessarily prove a match between corresponding views)

(ii) by output from a verification engine (e.g. Hercules) (note that this would prove a match between corresponding views)

This methodology, which gauges the "degree of diagonality" in a Schematic/Layout Block DMM, could be classified as being in the category of "Design-for-Layout".

Schematic Block - Design Engineer DMM
This would be generated manually to indicate the design engineer responsible for each particular schematic block.

Design Engineer - Design Engineer DSM
The Schematic Block – Design Engineer DMM information would then be combined with the Schematic Block – Schematic Block DSM to auto-generate a Design Engineer – Design Engineer DSM. The latter could be used to direct design sub-team formation and optimize the required design-related information flow.

Layout Block - Layout Engineer DMM
This would be generated manually to indicate the layout engineer responsible for each particular layout block.

Layout Engineer - Layout Engineer DSM
The Layout Block – Layout Engineer DMM information would then be combined with the Layout Block – Layout Block DSM to auto-generate a Layout Engineer – Layout Engineer DSM. The latter could be used to direct layout sub-team formation and optimize the required layout-related information flow.

Design Engineer - Layout Engineer DMM
By combining the information in three DMMs (Schematic Block – Layout Block, Schematic Block – Design Engineer, Layout Block – Layout Engineer), a Design Engineer – Layout Engineer DMM could be derived. The latter could be used to direct design/layout sub-team formation and optimize the required design/layout information flow.
In general, the MDM could be extended to include verification engineers, evaluation engineers, test engineers and other roles in the product development process.

To summarise the most salient and relevant design/layout information in one chart, a colour-coded "1.5D" Schematic/Layout DMM with "outer layers" of Design Engineers and Layout Engineers could be generated, as illustrated in Figure 5 [6].

"1.5D" DMM		Layout Engineers	Layout Engineer 1	Layout Engineer 2	Layout Engineer 3	Layout Engineer 4	Layout Engineer 5	Layout Engineer 6	Layout Engineer 7	Layout Engineer 8
		Layout Blocks	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7	Block 8
Design Engineers	Schematic Blocks									
Design Engineer 1	Block A		X							
Design Engineer 2	Block B			X	X					
Design Engineer 3	Block C		X		X					
Design Engineer 4	Block D			X	X	X				
Design Engineer 5	Block E						X			X
Design Engineer 6	Block F						X	X		
Design Engineer 7	Block G								X	
Design Engineer 8	Block H							X	X	X

Figure 5. "1.5D" Schematic/Layout DMM

3.2 Design & Simulation Verification

Another extension suggestion would be to include design simulations (and verification engineers) in the MDM, in which case, a Schematic Block – Design Simulation DMM could indicate missing or redundant simulations and could be used to aid simulation selection and prioritization.

Again, to summarise the most salient and relevant design/verification information in one chart, a colour-coded "1.5D" Schematic/Simulation DMM with "outer layers" of Design Engineers and Verification Engineers could be generated [6].

As well as the usual powerful visualisation of relationships/dependencies, DSM-directed chip design and verification would have the additional benefits of higher quality, due to the more rigorous, systematic approach, and more efficiency, due to the more focussed approach.

4 SUMMARY

The current approach to integrated circuit (I.C.), or chip, design and verification is limited in that it typically does not try to systematically optimise the schematic/layout hierarchy or, indeed, the project (sub-)team members' participation in terms of (sub-)block interface design and verification. This approach can lead to inefficient development execution and to simulation blindspots or omissions.

We can use the DSM, in an MDM methodology, to determine a more optimum schematic/layout hierarchy and a more optimum configuration of (sub-)team members and design/verification tasks, in a visually powerful way.

DSM-directed chip design and verification should be more efficient and of higher quality, as a consequence.

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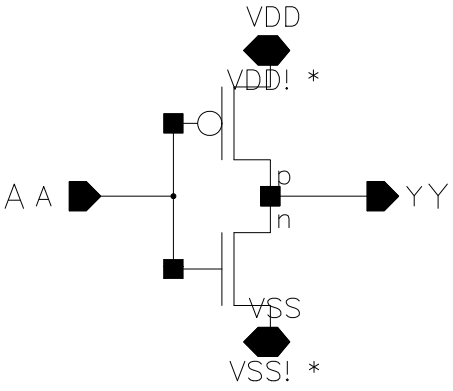
Introduction

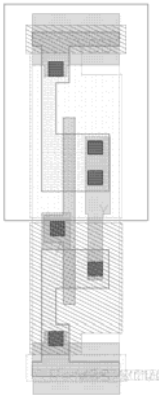
- The Current Approach to Integrated Circuit (I.C.), or Chip, development can be non-optimum in terms of “Design-for-Layout”
  - Non-optimum Schematic/Layout Hierarchy Creation
  - => Inefficient Development Execution
- The Current Approach can be non-optimum in terms of “Design-for-Verification”
  - Non-systematic Design/Verification Team Structure
  - => Limited Toplevel Simulation Checklist
- DSM/DMM/MDM methodology can potentially be used to
  - Ensure Optimised Schematic/Layout Hierarchy Creation
  - Determine a more Optimum Configuration of (sub-)Team Members and Design/Verification Tasks
- *DSM-directed* Chip Design & Verification should be more efficient and of higher quality

Current Chip Design & Verification Approach – Background

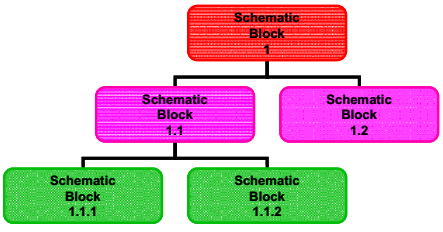
Schematic Block



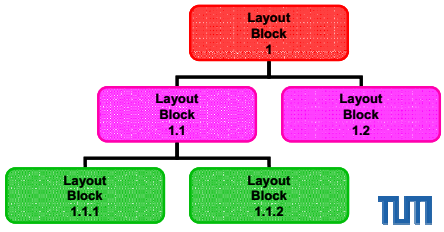
Layout Block



Schematic Hierarchy

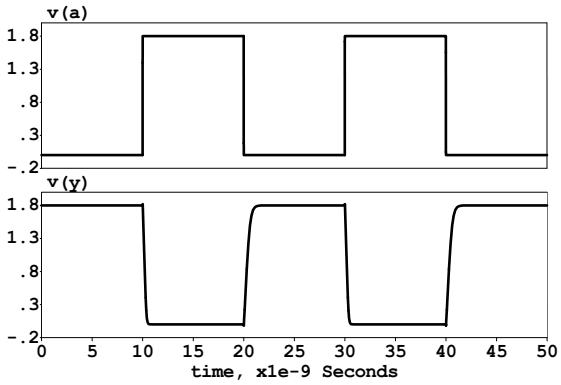


Layout Hierarchy

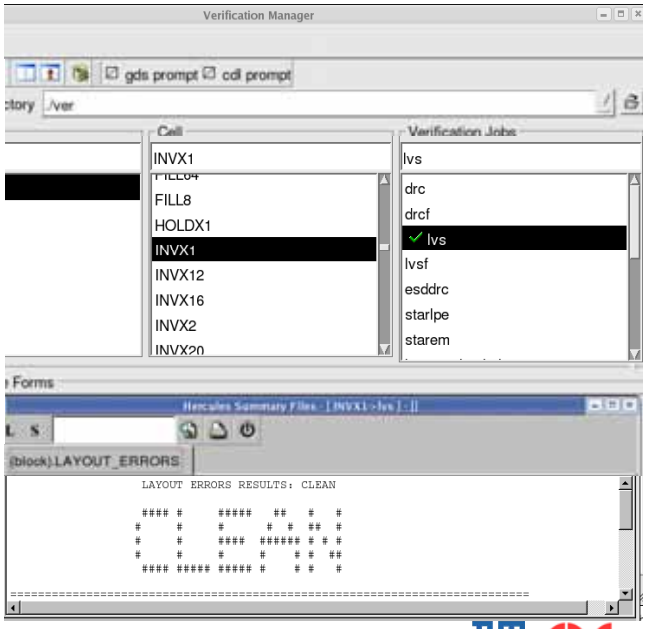


Current Chip Design & Verification Approach – Background

Simulation Verification



Layout-versus-Schematic (LVS) Verification



Current Chip Design & Verification Approach – Non-Optimum Aspects & Key Limitations

- Design & Layout
  - Ideally, there should be, as extensive as possible, one-to-one correspondence between the Schematic and Layout blocks in the chip database hierarchy
  - However, Design Engineers can often create the Schematics, in a hierarchy, without consideration for the Layout
  - Layout Engineers can often create the Layout, in a hierarchy, without consideration for the Design
  - => Limited one-to-one correspondence between the Schematic and Layout blocks in the chip database hierarchy
  - => Design/Layout can be time-consuming to create and verify (from a Layout-versus-Schematic, or LVS, perspective) successfully
- Design & Simulation Verification
  - Ideally, there should be a systematic approach to Defining Simulations (especially Toplevel) and Defining (sub-)Teams
  - However, Design Engineers can often be assigned to design/check their own block
  - Also, the Design/Verification Team structure tends not to take the Chip structure into account
  - => Non-systematic approach to Defining Simulations (especially Toplevel) and Defining (sub-)Teams
  - => Toplevel Chip Simulation checklist can be too limited, with simulation "blindspots" or omissions

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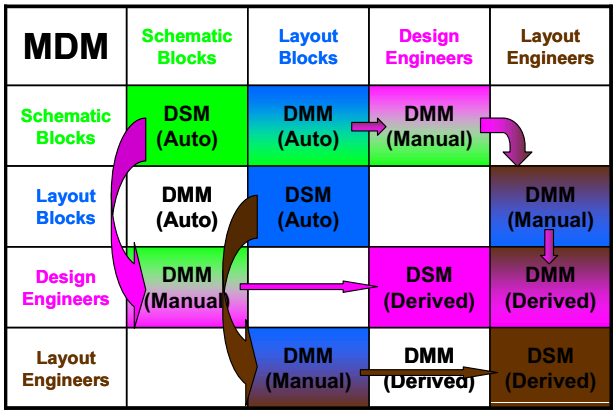
New Chip Design & Verification Approach – Design & Layout MDM



- Suggested use of an Multi-Domain-Matrix (MDM) approach to systematically improve Design/Layout process
- Schematic Block / Layout Block DSMs/DMMs could be automatically generated
- Schematic Block / Design Engineer, Layout Block / Layout Engineer DMMs could be manually generated
- Design Engineer / Layout Engineer DSMs/DMMs could be then derived

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New Chip Design & Verification Approach – Schematic/Layout Block DSMs

- Schematic Block – Schematic Block DSM would illustrate the degree of connectivity between the schematic blocks
- Layout Block – Layout Block DSM would illustrate the degree of connectivity between the layout blocks
- Clustering of these DSMs could suggest a better hierarchy (i.e. partitioning) for the schematics and layout
- In cases where the current schematic or layout hierarchy cannot be changed, a new approach, called “Virtual Clustering” (or virtual partitioning) could be used

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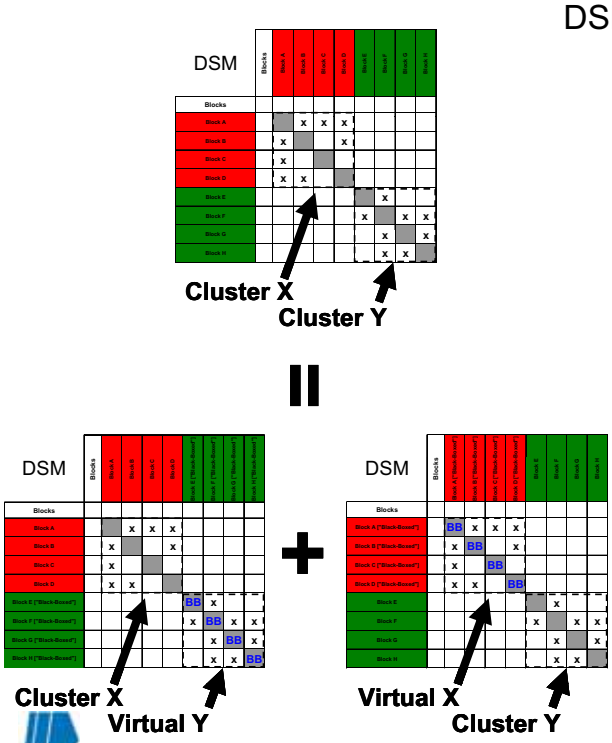
New Chip Design & Verification Approach – Schematic/Layout Block DSMs



- Concept of "Virtual Clustering"
- Current hierarchy is not changed
- Schematic/Layout elements, outside the cluster of immediate interest, would be "black-boxed"
- Key benefit would be reduction in the size of the schematic/layout data for more efficient verification analysis
- This methodology could be classified as being in the "Design-for-Verification" category

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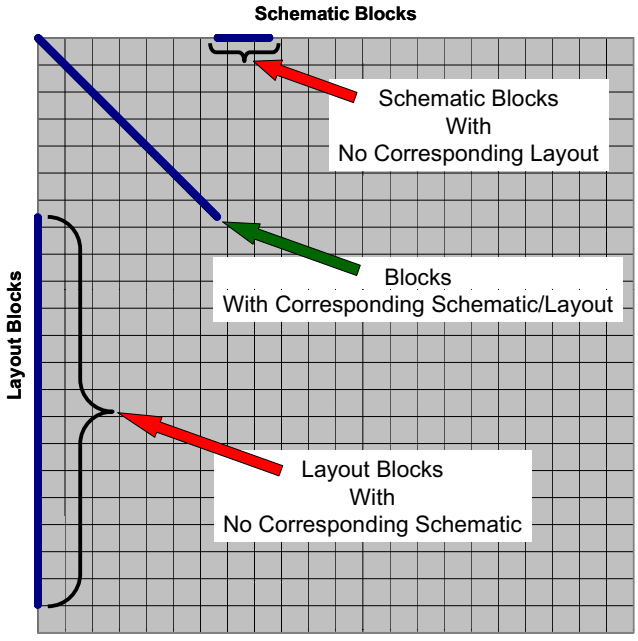
New Chip Design & Verification Approach – Schematic/Layout Block DMMs/DSMs



- Concept of "Diagonality"
- Schematic Block – Layout Block DMM would illustrate the degree of correspondence between Schematic Blocks and Layout Blocks in the Chip Database hierarchy
  - 2,291 Blocks in Example shown
- Should ideally be mostly diagonal, indicating a one-to-one relationship between a schematic block and its corresponding layout block

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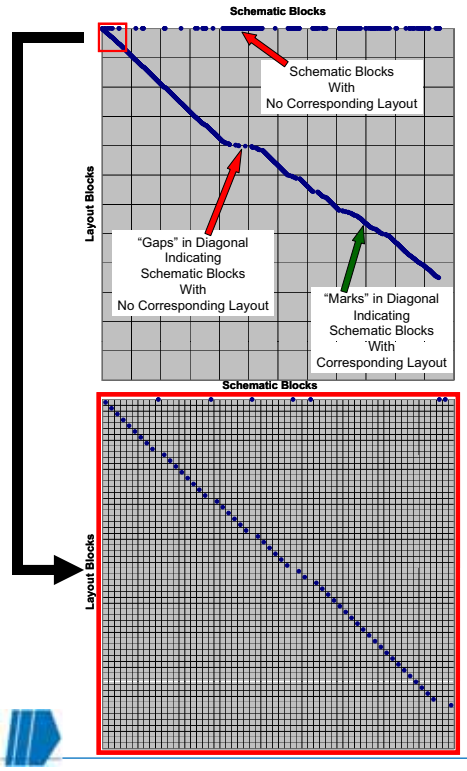
New Chip Design & Verification Approach – Schematic/Layout Block DMMs/DSMs



- Concept of "Diagonality"
- Schematic Block – Layout Block DMM
  - 1,152 Blocks (60 Block zoom-in)
- Automatically generated from a Design Schematic Netlist and Design/Layout Library
- Re-ordered by Hierarchy
- "Mark" in Diagonal indicates a Schematic Block with Corresponding Layout
- "Gap" or "Flattening" in Diagonal indicates a Schematic Block with No Corresponding Layout

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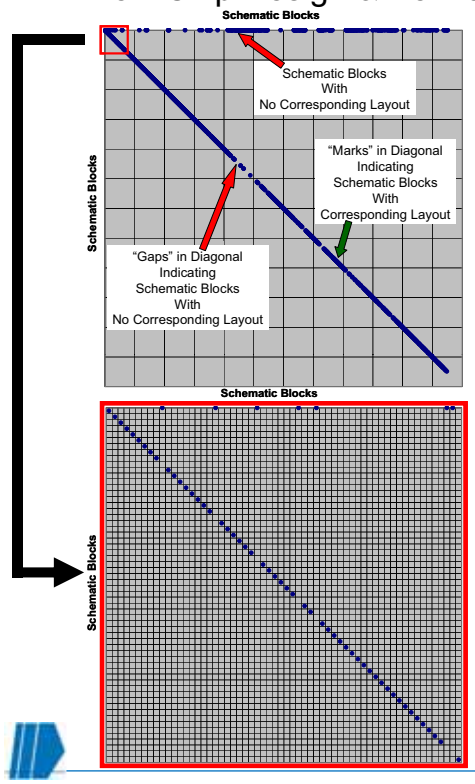
New Chip Design & Verification Approach – Schematic/Layout Block DMMs/DSMs



- Concept of "Diagonality"
- Schematic Block – Schematic Block DSM
  - 1,152 Blocks (60 Block zoom-in)
- Automatically generated from a Design Schematic Netlist and Design/Layout Library
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- "Mark" in Diagonal indicates a Schematic Block with Corresponding Layout
- "Gap" in Diagonal indicates a Schematic Block with No Corresponding Layout

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New Chip Design & Verification Approach – Overall "1.5D" DMM

"1.5D" DMM

Design Engineers	Schematic Blocks	Layout Engineers	Layout Engineer 1	Layout Engineer 2	Layout Engineer 3	Layout Engineer 4	Layout Engineer 5	Layout Engineer 6	Layout Engineer 7	Layout Engineer 8
		Layout Blocks	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7	Block 8
Design Engineer 1	Block A		x							
Design Engineer 2	Block B			x	x					
Design Engineer 3	Block C		x		x					
Design Engineer 4	Block D			x	x	x				
Design Engineer 5	Block E						x			x
Design Engineer 6	Block F						x	x		
Design Engineer 7	Block G								x	
Design Engineer 8	Block H							x	x	x

- Overall "1.5D" DMM
- Schematic / Layout DMM with "outer layers" of Design Engineers and Layout Engineers
- Summarises the most salient and relevant design/layout information in one chart

New Chip Design & Verification Approach – Design & Simulation Verification

MDM	Schematic Blocks	Simulations	Design Engineers	Verification Engineers
Schematic Blocks	DSM (Auto)	DMM (Auto)	DMM (Manual)	
Simulations	DMM (Auto)	DSM (Auto)		DMM (Manual)
Design Engineers	DMM (Manual)		DSM (Derived)	DMM (Derived)
Verification Engineers		DMM (Manual)	DMM (Derived)	DSM (Derived)

"1.5D" DMM

Design Engineers	Schematic Blocks	Verification Engineers	Verification Engineer 1	Verification Engineer 2	Verification Engineer 3	Verification Engineer 4	Verification Engineer 5	Verification Engineer 6	Verification Engineer 7	Verification Engineer 8
		Simulations	Simulation 1	Simulation 2	Simulation 3	Simulation 4	Simulation 5	Simulation 6	Simulation 7	Simulation 8
Design Engineer 1	Block A		x							
Design Engineer 2	Block B			x	x					
Design Engineer 3	Block C		x		x					
Design Engineer 4	Block D			x	x	x				
Design Engineer 5	Block E						x			x
Design Engineer 6	Block F						x	x		
Design Engineer 7	Block G								x	
Design Engineer 8	Block H							x	x	x

- Design & Simulation Verification
- Include Design Simulations and Verification Engineers in the MDM
- Schematic Block – Design Simulation DMM could indicate missing or redundant simulations
- Could be used to aid simulation selection and prioritisation
- Schematic / Simulation DMM with "outer layers" of Design Engineers and Verification Engineers
- Summarises the most salient and relevant design/verification information in one chart

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New Chip Design & Verification Approach – Key Benefits

- Design & Layout
  - "Virtual Clustering" and "Black-Boxing"
  - => reduction in size of Schematic / Layout data for more efficient verification analysis
  - "Diagonality"
  - => illustrates the degree of correspondence between Schematic Blocks and Layout Blocks in the Chip Database hierarchy
  - => ensures optimised schematic/layout hierarchy creation
- Design & Simulation Verification
  - Higher Quality,due to the more rigorous systematic approach
  - More Efficiency, due to the more focussed approach

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Summary

- The Current Approach to Integrated Circuit (I.C.), or Chip, development can be non-optimum in terms of "Design-for-Layout"
  - Non-optimum Schematic/Layout Hierarchy Creation
  - => Inefficient Development Execution
- The Current Approach can be non-optimum in terms of "Design-for-Verification"
  - Non-systematic Design/Verification Team Structure
  - => Limited Toplevel Simulation Checklist
- DSM/DMM/MDM methodology can potentially be used to
  - Ensure Optimised Schematic/Layout Hierarchy Creation
  - Determine a more Optimum Configuration of (sub-)Team Members and Design/Verification Tasks
- *DSM-directed* Chip Design & Verification should be more efficient and of higher quality